Application Note
Solution of Flickering in TFT

Contents

Application Notes on LCD's Flickering (TFT Series)

1 Introduction

Flickering is the opposing changes in intensity of luminosity periodically that can be observed by human eyes. This is usually caused by flashing, or contrast patterns that oscillate at a frequency which makes viewers believe the image is moving or changing. In TFT module design, there are different causes for this issue and can be avoided with various techniques in TFT panel and driver IC design.

2 Flickering Causes

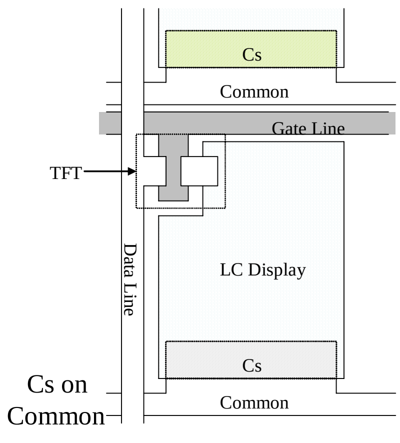
Here are some critical areas that may lead to flickering.

a. Unstable power supply
b. Un-matched gamma in Positive and Negative frame
c. Low refresh rate
d. Un-optimized Vcom level

3 Illustrations

3.1 Unstable Power Supply

- Figure 3-1 shows the basic pixel structure in the TFT panels.
- The equivalent circuit model is shown in Figure 3-2.
- Voltage applies to the LC (Vlc) is controlled by the Vgate, Vsource and Vcom. When Vgate is driven to high, source voltage (Vsource) is applied to the LC display with respect to Vcom as shown in Figure 3-2.
- Figure 3-3 shows the ideal voltage level of the control signals in the positive and negative frame for the same color. Notice that the Vlc is equal to the differences between the Vsource and Vcom and should be unchanged for the same color level in the positive and negative frame.
- Figure 3-4 shows an example that the Vsource level is affected when data is written into the memory in video mode. In this example, the video data transmission frequency is 30Hz and the frame frequency is 60Hz. Video data will be transmitted and induced a peak current switching periodically in the negative frame. If the ITO resistance is too high and the power supply is unstable, Vlc will be affected and became unmatched in positive and negative frame. Flickering will occur if this happens periodically.



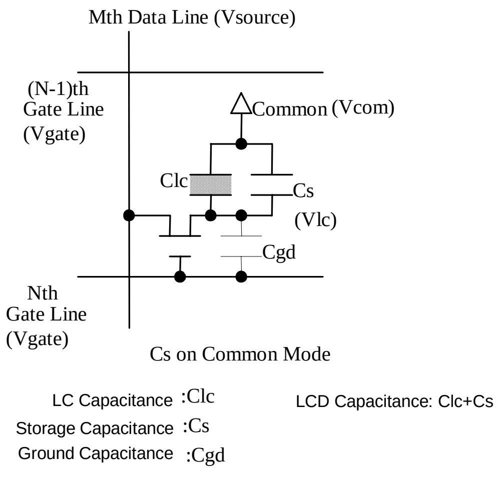


Figure 3-1 Pixel Structure in TFT Panel	**Figure 3-2 Pixel circuit model in TFT Panel**

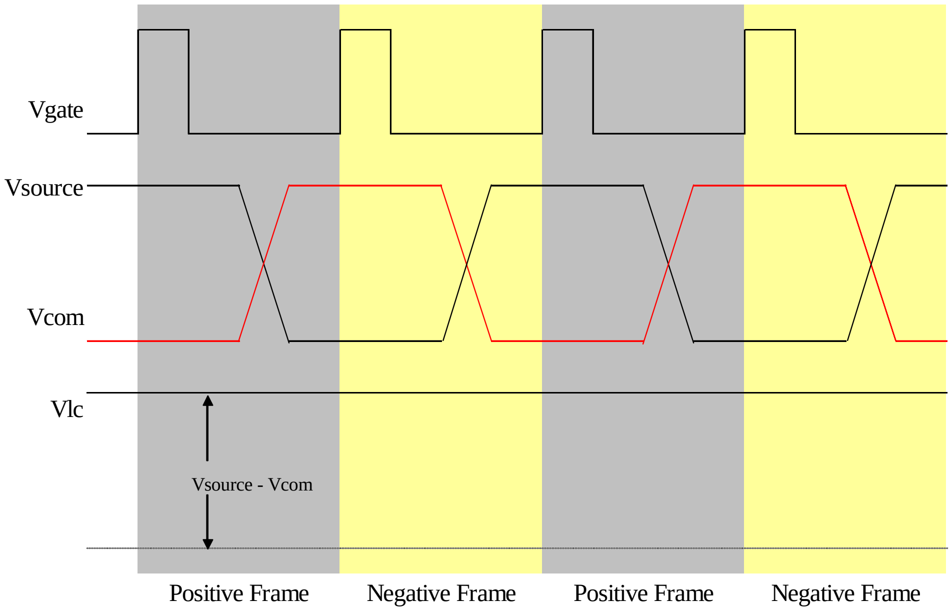


Figure 3-3 Ideal Vsource and Vcom Voltage Level at Same Pixel during Positive and Negative Frame

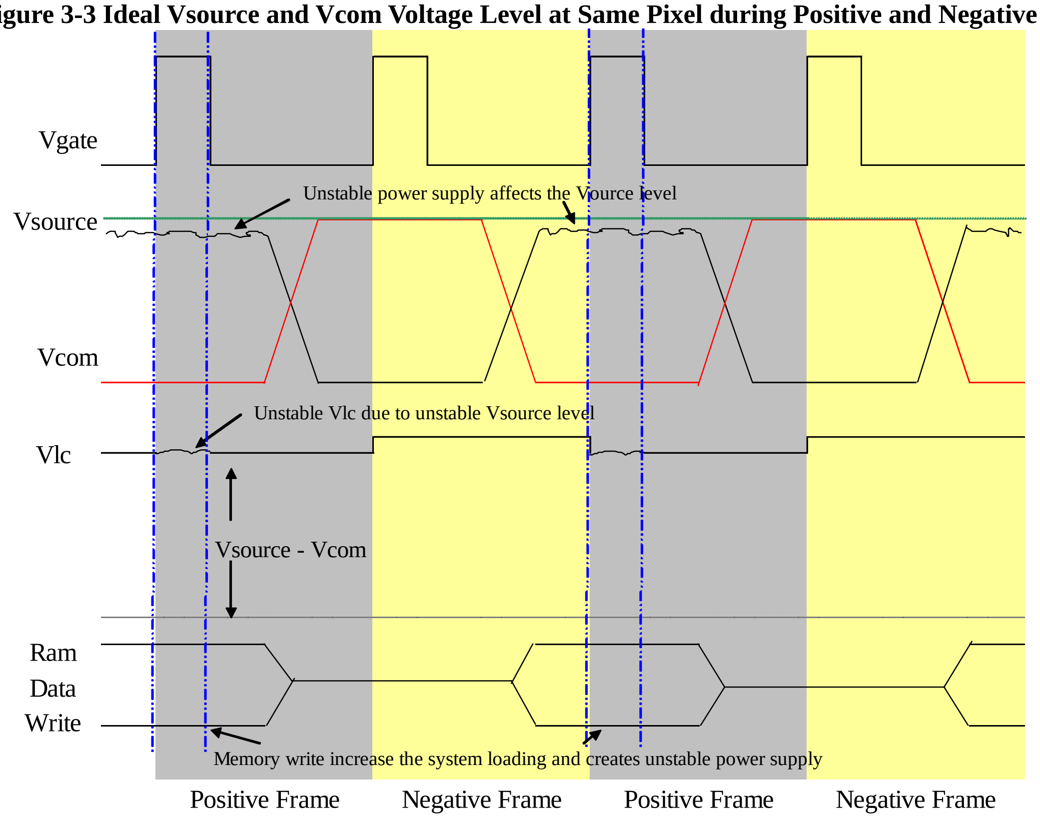


Figure 3-4 Abnormal Vsource Level at Same Pixel during Positive and Negative Frame due to Unstable Power

3.2 Un-matched Gamma in Positive and Negative Frame

- Figure 3-5 shows the ideal Vsource level (V0-V7) at different gray scale voltage in the positive and negative frame with AC Vcom.
- Same color will be displayed when the voltage level of V0 in the positive frame and the negative frame is the same. If they are mismatched, LC voltage will be affected as shown in Figure 3-6 and flickering occurs.
- Gamma is used to measure the luminance against the grey scale level voltage.
- Ideally both gamma curves of the positive and negative frame should be the same if the gray scale voltage is matched. If they are mismatched, the gamma curves are different as shown in Figure 3-7.

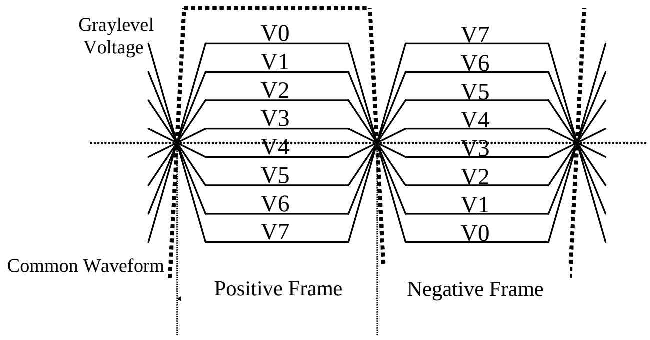


Figure 3-5 Gray Scale Level

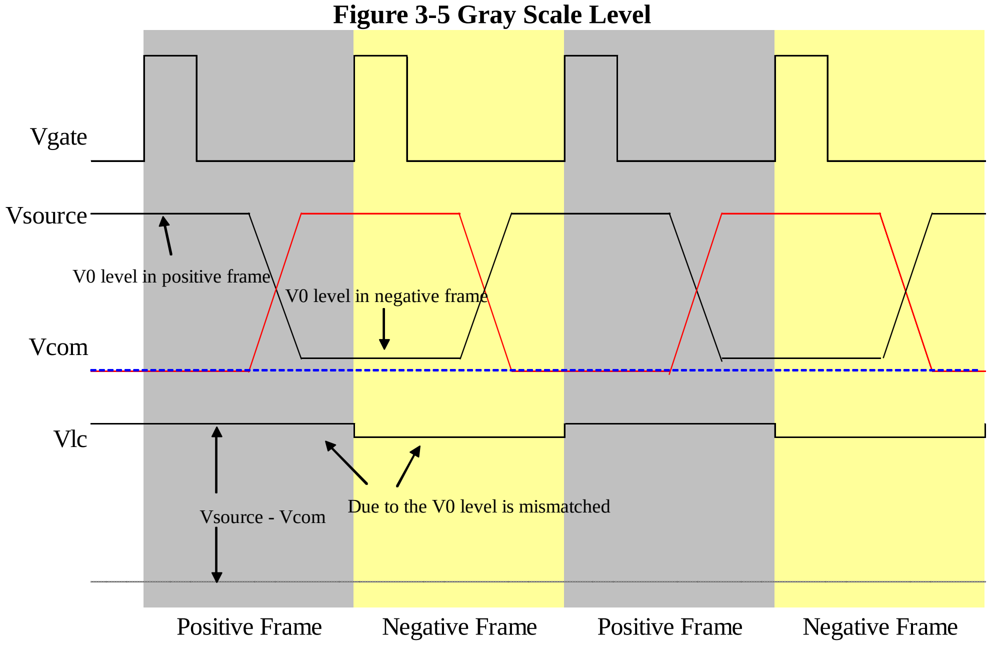


Figure 3-6 Un-matched Vsource Level due to Un-tuned Gamma

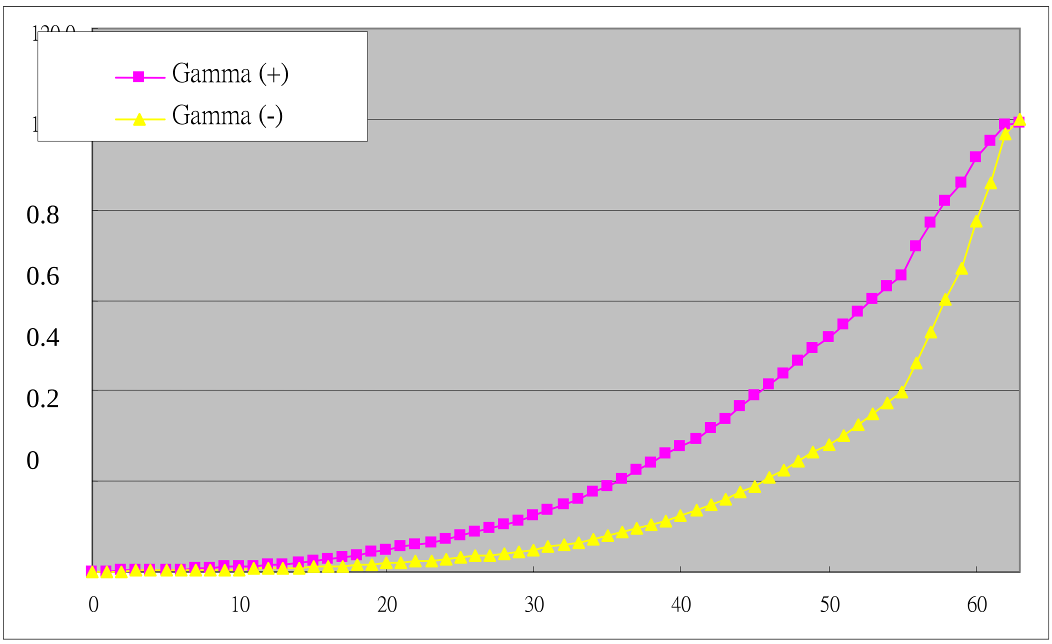


Figure 3-7 Gamma Curve of Unmatched Positive and Negative Frame

- With different inversion schemes as shown in Figure 3-8, the severity of the flickering will be different.
- '+' and '-' represent the polarity of the Vsource level as shown in the positive frame in Figure 3-6.

- In Frame inversion, the polarity of the Vsource of the whole panel is the same in each frame and will switch polarity in every frame. Flickering becomes noticeable by the customers if positive and negative frame is mismatched. This kind of flickering is “Frame Flickering”.
- In Line inversion and column inversion, the polarities of the row and the column Vsource are different respectively in each frame. If the positive and negative frame is mismatched, the whole row or column of line will appear moving to the viewers. This kind of flickering is “Line Flickering”.
- In Dot Inversion scheme, each pixel is displayed in different polarity in each frame and flickering is less noticeable if it is mismatched in the positive and negative frame.

Frame Inversion

Frame N (Columns)

Lines	1	2	3	4	5
1	+	+	+	+	+
2	+	+	+	+	+
3	+	+	+	+	+
4	+	+	+	+	+
5	+	+	+	+	+

Frame N+1 (Columns)

Lines	1	2	3	4	5
1	-	-	-	-	-
2	-	-	-	-	-
3	-	-	-	-	-
4	-	-	-	-	-
5	-	-	-	-	-

Row Inversion

Frame N (Columns)

Lines	1	2	3	4	5
1	+	+	+	+	+
2	-	-	-	-	-
3	+	+	+	+	+
4	-	-	-	-	-
5	+	+	+	+	+

Frame N+1 (Columns)

Lines	1	2	3	4	5
1	-	-	-	-	-
2	+	+	+	+	+
3	-	-	-	-	-
4	+	+	+	+	+
5	-	-	-	-	-

Column Inversion

Frame N (Columns)

Lines	1	2	3	4	5
1	+	-	+	-	+
2	+	-	+	-	+
3	+	-	+	-	+
4	+	-	+	-	+
5	+	-	+	-	+

Frame N+1 (Columns)

Lines	1	2	3	4	5
1	-	+	-	+	-
2	-	+	-	+	-
3	-	+	-	+	-
4	-	+	-	+	-
5	-	+	-	+	-

Dot Inversion

Frame N (Columns)

Lines	1	2	3	4	5
1	+	-	+	-	+
2	-	+	-	+	-
3	+	-	+	-	+
4	-	+	-	+	-
5	+	-	+	-	+

Frame N+1 (Columns)

Lines	1	2	3	4	5
1	-	+	-	+	-
2	+	-	+	-	+
3	-	+	-	+	-
4	+	-	+	-	+
5	+	-	+	-	+

Figure 3-8 Various Inversion Schemes

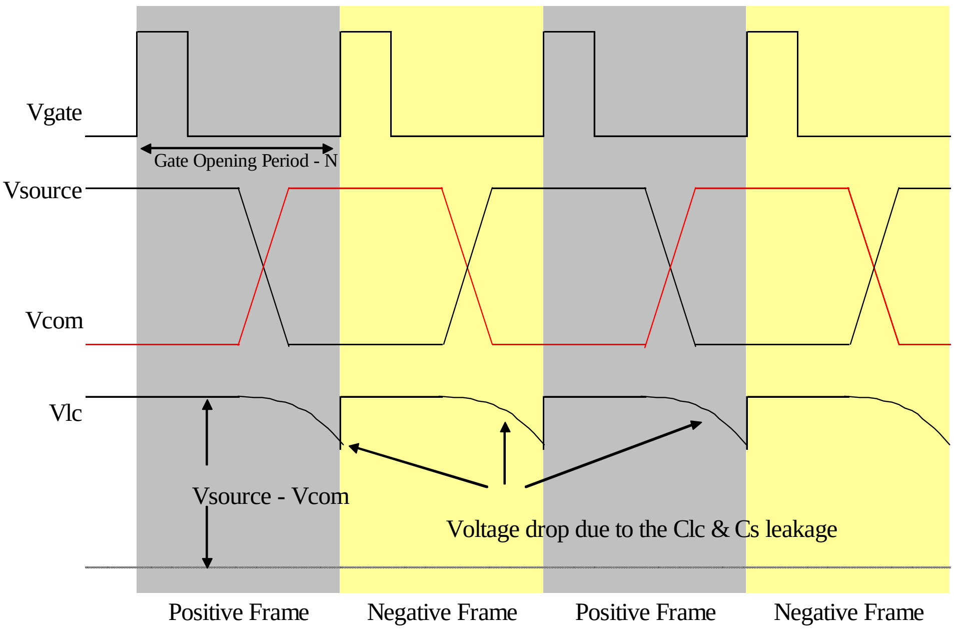


Figure 3-9 LC Voltage drop due to Clc Leakage

3.3 Low Refresh rate

- Refresh rate controls the frequency of the gate opening (N). When the gate opens, source voltage is applied to the source line of LCD and charges up the Clc and Cst to show the color. Once the gate is closed, the color will depend on the charged up value of the capacitors, LC capacitor (Clc) and Storage Capacitor (Cs) as shown in Figure 3-2.
- Clc & Cs will have a leakage current in the gate closing period. Moreover, there is a device leakage current from the source to the drain of the transistor and it is panel-by-panel based. If the refresh rate is low or device leakage is large, the leakage current will be significant enough to affect the voltage on LC. Once the gate is activated, the Clc and Cs is charged up again as shown in Figure 3-9. Flickering occurs due to this voltage drops.

3.4 Un-optimized Vcom level

- As shown in Figure 3-3, the gray scale level is depended on the applied LC voltage (Vsource –Vcom).
- Due to the offset within each LCD panel, the required Vcom voltage can be slightly differ.
- This offset can cause the unmatched LC voltage in the positive and negative frame as shown in Figure 3-10 and create the appearance of flicker within the display.

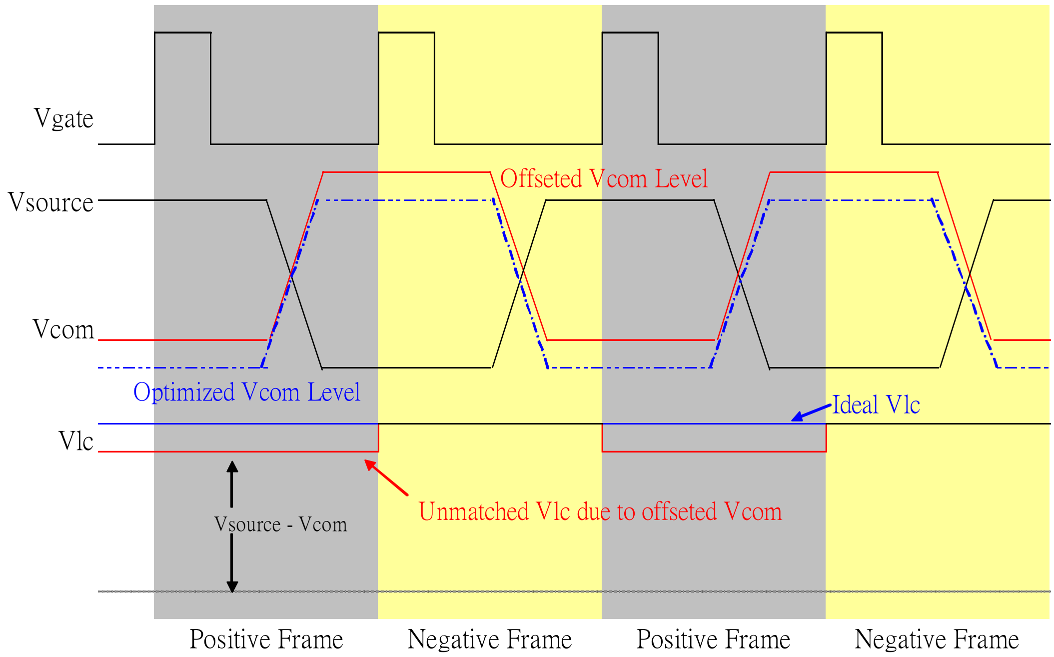


Figure 3-10 Un-optimized Vcom Level

3 Improvements

4.1 Driver Level

VCIX3 Power Architecture

- In the future, SSL TFT driver products will be added VCIX3 as reference to generate Vcom waveform. This increases Vcom voltage level stability, especially in high loading panel. (panel size >3.5 inch).
- In these drivers, VCIX3 is also the source to generate VLCD. More stable VLCD will increase source voltage reference output stability. This minimizes source voltage output distortion in high loading pattern (e.g. plain grey).

Gamma Control

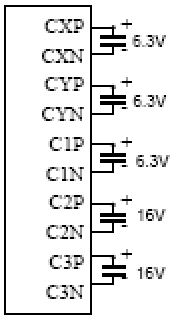
- In SSL TFT driver products, user command set for gamma control is provided. User can use these to tune the gamma curve of the positive and negative frame and eliminate the flickering. Driver ICs with various inversion schemes are also available, e.g. SSD2220, SSD1297 with line inversion, SSD2125 with dot inversion for user to choose based on their application needed.

VCOM Level Turning

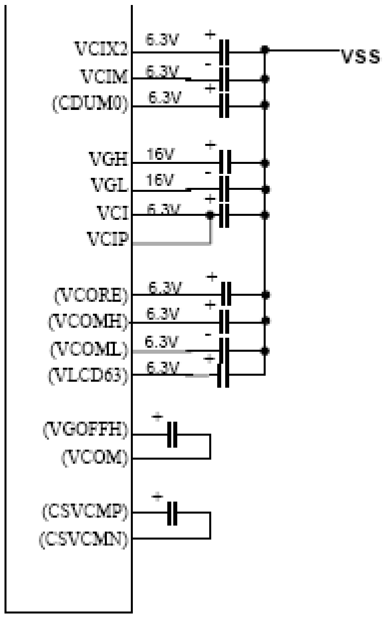
- Adjust the Vcomh level on the panel-by-panel can eliminate the flickering. In SSL TFT driver products (e.g. SSD2118, SSD2123), Multiple-Time Programming (MTP) function and user command sets are provided to user to tune the Vcomh value.

4.2 Panel Level

- Maximum supply power can be achieved by careful ITO layout and decreasing the ITO resistance. Suggested ITO resistance of the power pin (e.g. VCI, VCIX2) should be less than or equal to 5 ohms. Increasing the power pin counts and pad width is also recommended. Figure 3-2 below shows an example of ITO resistance requirement on input pins.
- Stable power supply can be achieved by using the appropriated capacitors on the FPC. In SSL TFT drivers, recommended capacitors values are stated in the datasheet for the best performance as shown in Figure 3-1.



All capacitors
0.1 ~ 0.22uF (0.22uF for better stability)



Mandatory requirement on external components for SSD1269 is 10 capacitors.
VCIX2, VCIM, VGH, VGL, VCI, C1P/C1N, C2P/C2N, C3P/C3N, CXP/CXN, CYP/CYN

Remark:
Capacitor for VCIX2 = 2.2uF
VCI should be separated with VCIP at ITO layout to provide noise free path.
VSS should be separated with VCHS, AVSS and VSSRC at ITO layout to provide noise free path.
All other capacitors 1.0uF ~ 2.2uF (2.2uF is preferred for better display quality and power consumption.)

(Optional capacitors)
Two or more capacitors on VREGC/VCORE are optional which depends on application.
VCOMH, VCOML, VLCD63, capacitors are for stability
Capacitors on CDUM0, CSVCMP, CSVCMN are for power saving.
Capacitors on VGOFFHL/VCOM are for Cs on gate. . Leave them open for Cs on COM application.

Pins	Recommended Capacitor Value
VCIX2	2.2uF
VCIM	1.0~2.2uF
VGH	1.0~2.2uF
VGL	1.0~2.2uF
VCI	1.0~2.2uF
C1N/C1P	0.1~0.22uF
C2N/C2P	0.1~0.22uF
C3N/C3P	0.1~0.22uF
CXN/CXP	0.1~0.22uF
CYN/CYP	0.1~0.22uF

Figure 3-1 Recommended Capacitors Values

Pins	Recommended ITO Resistance
VCIX2	5 OHM
VCI	5 OHM
VGH	10 OHM
VGL	10 OHM
VCIM	10 OHM
VCOMH	5 OHM
VCOML	5 OHM
VCHS	5 OHM

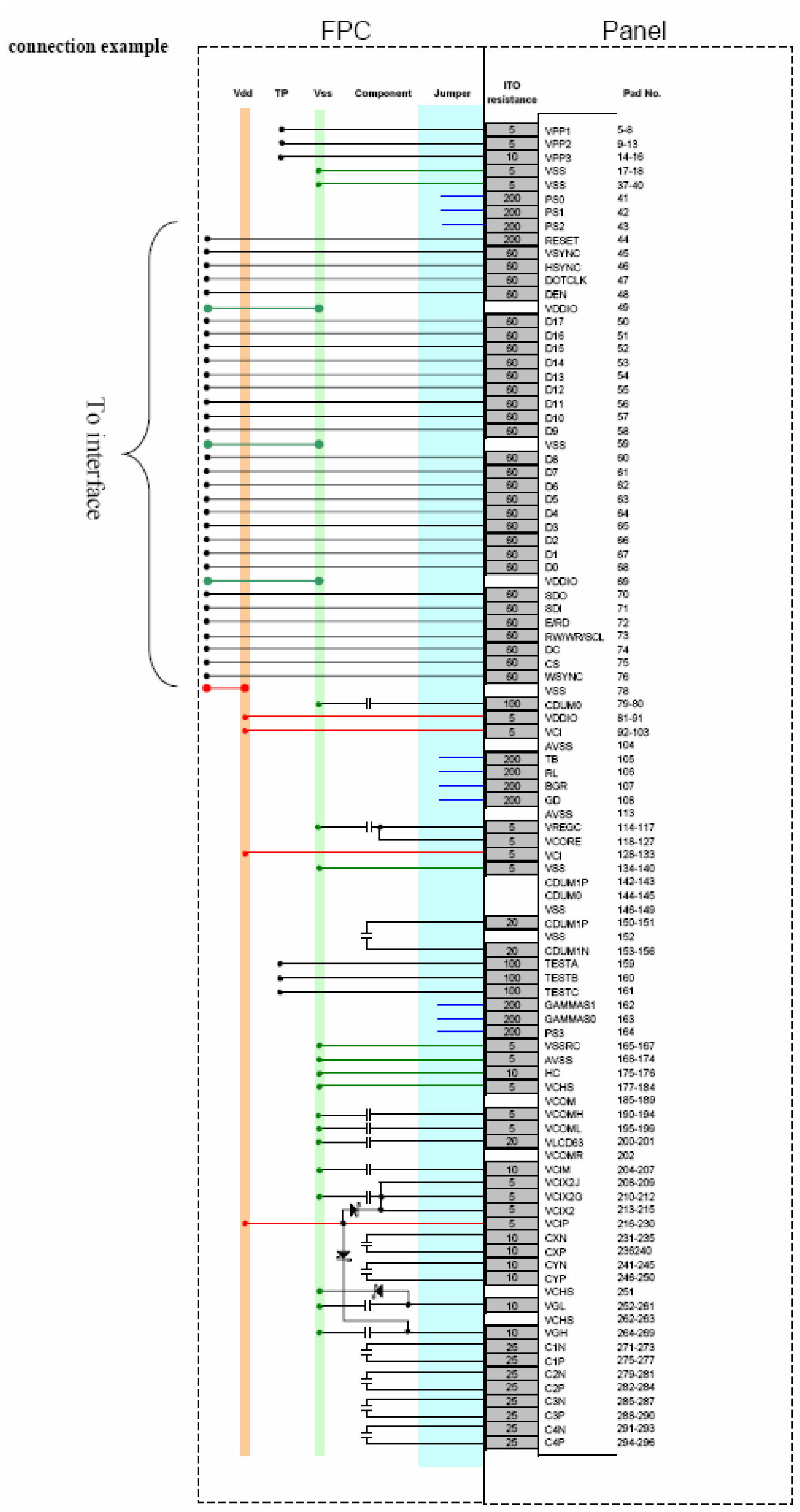


Figure 3-2 Recommended ITO Resistance