

*Application Note*  
*Solution of Crosstalk in TFT*

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## Application notes on CROSSTALK (TFT SERIES)

### 1. Background

Crosstalk in general is a visual defect that causes contrast difference in some areas of display which display the same grayscale. It occurs because of the interference caused by adjacent pixels.

Because there are transistors to isolate its pixel from data lines in non-select period per frame, TFT panels have a better performance on crosstalk when compared with STN/CSTN panel.

### 2. Root causes

#### 2.1. *Driver IC dependence*

There are mainly three driver IC dependent parameters which may cause crosstalk.

- Driving strength of VCOM pin.
  - i. Reference voltage (VCIX2) for VCOM level generation is not strong enough. VCOM level is distorted when data lines are toggling.
- Driver IC VCOM pin output resistance on VCOMH/VCOML level output ( $R_{on}$  in Fig 1)
  - i. Larger output resistance of VCOM pin causes larger RC between sources & VCOM
- Driving strength of reference analog buffer voltage output (VLCD) from source pins.
  - i. In some display patterns, all pixels in the same scan line are displaying same gray level. Sources output loading are increased and so cause distortion in output level when compare with other scan lines which are displaying different grey level.

#### 2.2. *Panel Dependence*

There are mainly three panel dependent parameters which may cause crosstalk.

- Parasitic capacitance between VCOM & Source ( $C_1$  in Fig 1)
  - i. This parasitic capacitance causes larger RC between Source & VCOM.
- Parasitic capacitance between pixel electrode & Source ( $C_2$  in Fig 1)
  - i. This parasitic capacitance causes coupling of source signal to pixel electrode even in non-selection period of a frame.
- Resistance of ITO layout of VCOM & Source ( $R_{sheet}, R_{ITO}$  in Fig 1)
  - i. This parasitic resistance causes larger RC between Source & VCOM.

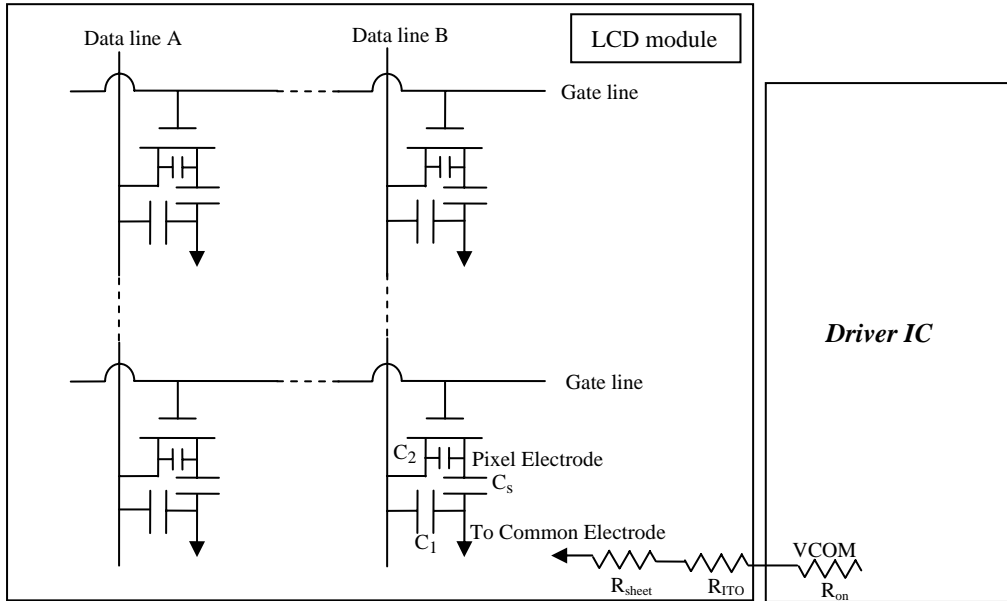


Fig 1: Equivalent circuit of LCD module (Cs on common) & Driver IC

### 3. Illustration

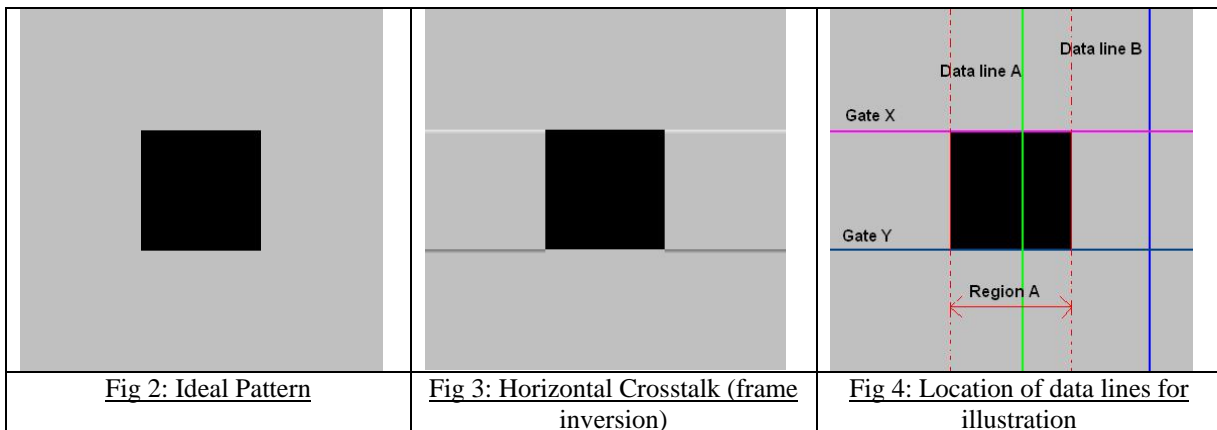
There are mainly two kinds of crosstalk, horizontal crosstalk & vertical crosstalk. Below examples are assumed to use normally white, Cs on common & DC VCOM driving scheme.

#### 3.1. Horizontal Crosstalk

- Horizontal crosstalk is mainly caused by common electrode signal distortion.
- This distortion is caused by capacitive coupling between the data-lines (Source) and common sheet electrode (VCOM) through a parasitic capacitor ( $C_1$  in Fig 1) in TFT LCD.

##### 3.1.1. Effect of parasitic capacitance ( $C_1$ ) on VCOM

###### 3.1.1.1. Frame inversion



- Fig.2 pattern is usually used for crosstalk evaluation.
- Fig.3 shows display affected by horizontal crosstalk (frame inversion)
- Fig.4 shows region A, data line location A,B and gate X,Y which are used for illustration
- Fig.5 shows data line A, B & VCOM signal waveform.
- At Time T1, Frame starts with gray pixels.
- At Time T2, voltage of all data lines in Region A (e.g. Data line A) goes upward (at upper edge of the black box in display pattern).

- These distort VCOM level (highlighted in RED in Fig.5) through parasitic capacitance  $C_1$
- In between T2 & T3, gate X is turned ON to charge up all storage capacitor  $C_s$  lined on gate X to voltage level ( $V_{source} - V_{COM}$ ).
- $V_{COM}$  level cannot recovers to its normal value when gate X is turned off at time T3. Therefore, final voltage across charged  $C_s$  is smaller than expected.
- Hence lighter gray tone appears on pixels along gate X (Fig. 3) assuming that normally white panel is used.
- Vice versa in Time T4 & T5, voltage across  $C_s$  on gate Y pixels is larger than expected. Darker gray tone appears on pixels along gate Y.

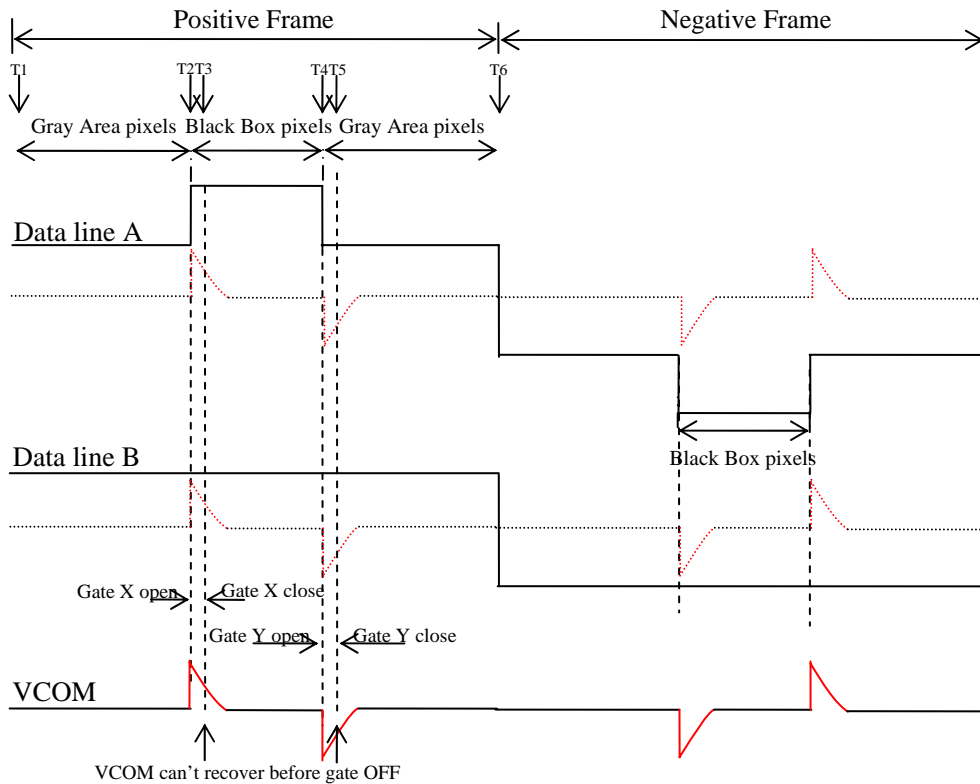
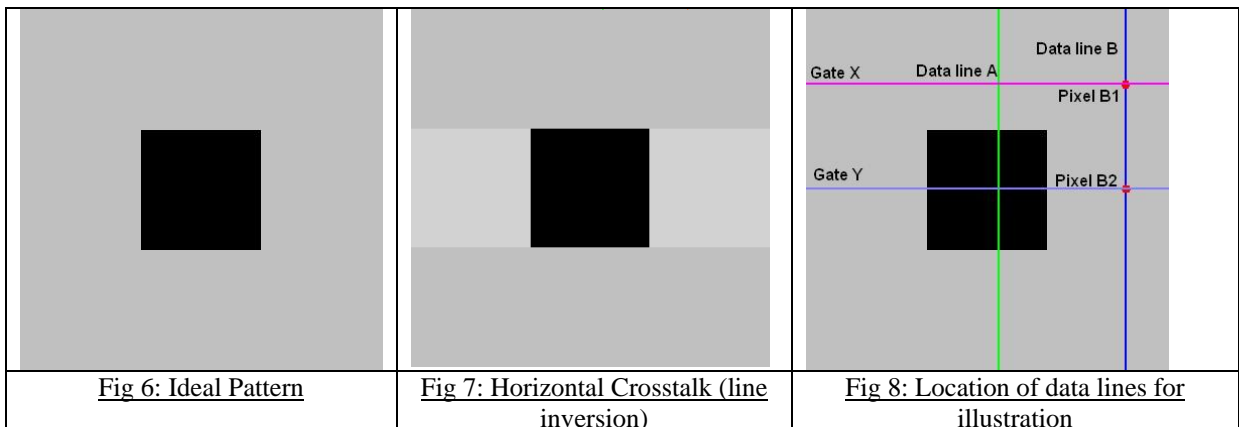


Fig 5: VCOM signal distorted by data line A (frame inversion)

### 3.1.1.2. 1-line inversion



- Fig.6 pattern is the ideal pattern without crosstalk effect.
- Fig.7 shows display affected by horizontal crosstalk (line inversion)
- Fig.8 shows data line location A & B, gate X & Y which are used to illustrate horizontal crosstalk.

- Fig.9 shows data line A, B & VCOM signal waveform
- Data line voltage toggles per line instead of on edge on black box.
- In gray area pixel region (e.g. pixel B1 in gate X), Data line output voltage swing is small.
- Distorted  $V_{COM}$  level can recover to normal level before every gate OFF. Therefore, voltage across  $C_s$  haven't been affected in this area.
- In black box pixel region (e.g. pixel B2 in gate Y), Data line output voltage swing is large.
- Distorted  $V_{COM}$  cannot recover to normal before gate OFF. Therefore, voltage across  $C_s$  ( $V_{source}-V_{COM}$ ) is smaller than expected. Lighter gray tone appears on that region.

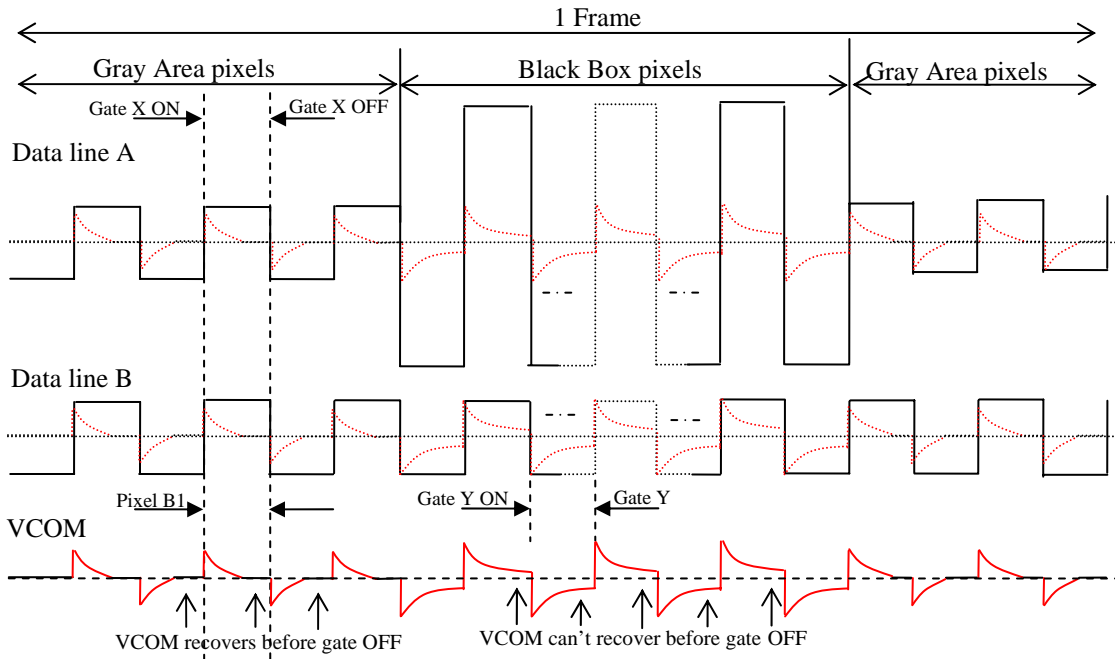


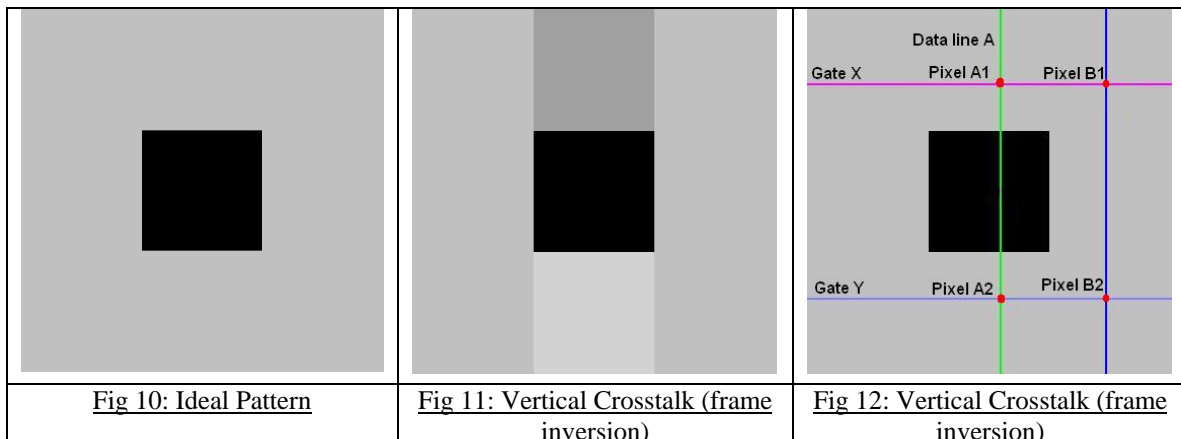
Fig 9: VCOM signal distorted by data line A (line inversion)

### 3.2. Vertical Crosstalk

- Vertical Crosstalk is mainly caused by the parasitic capacitance between the column or data line and the liquid-crystal pixel electrode. ( $C_2$  in Fig 1)
- Information intended for a picture element on a column is coupled into other picture elements on that column and adjacent columns.
- Even though the transistor connecting the data line to the pixel electrode may be turned off, the parasitic capacitance causes a fraction of the data voltage to appear on the pixel electrode, that is, across the liquid crystal pixel.

#### 3.2.1. Effect of parasitic capacitance ( $C_2$ ) on pixel electrode

##### 3.2.1.1. Frame Inversion



- Fig.10 pattern is the ideal pattern without crosstalk effect.
- Fig.11 shows display which is affected by vertical crosstalk (frame inversion)
- Fig.12 shows data line A, B, pixel A1, A2, B1 & B2 location which are used to illustrate vertical crosstalk.
- Fig.13 shows pixel A1 & pixel A2 electrode voltage which are affected by Data line A
- At time  $T_0$ , gate X is turned ON.  $C_s$  on pixel A1,B1 are charged up. Voltage on pixel electrode of pixel A1 becomes the same voltage as in data line A; pixel B1 becomes the same voltage as in data line B.
- At time  $T_1$ , gate X is turned OFF. Ideally, there should not be any changes in voltage level of pixel electrode A1, B1 until gate X is turned ON again at time  $T_7$ .
- At time  $T_2$ , changes in voltage level of data line A are coupled to pixel electrode A1 & A2 through parasitic capacitance  $C_2$ , even though gate X has been turned OFF.
- For pixel B1 & B2, because there is no change in voltage level of data line B, voltage on pixel electrode B1 is not affected.
- RMS voltage of pixel A1 is higher than that of pixel B1. Therefore, region A1 appears to be darker than Region B1.
- RMS voltage of pixel A2 is lower than that of pixel B2. Therefore, region A2 appears to be lighter than Region B2.

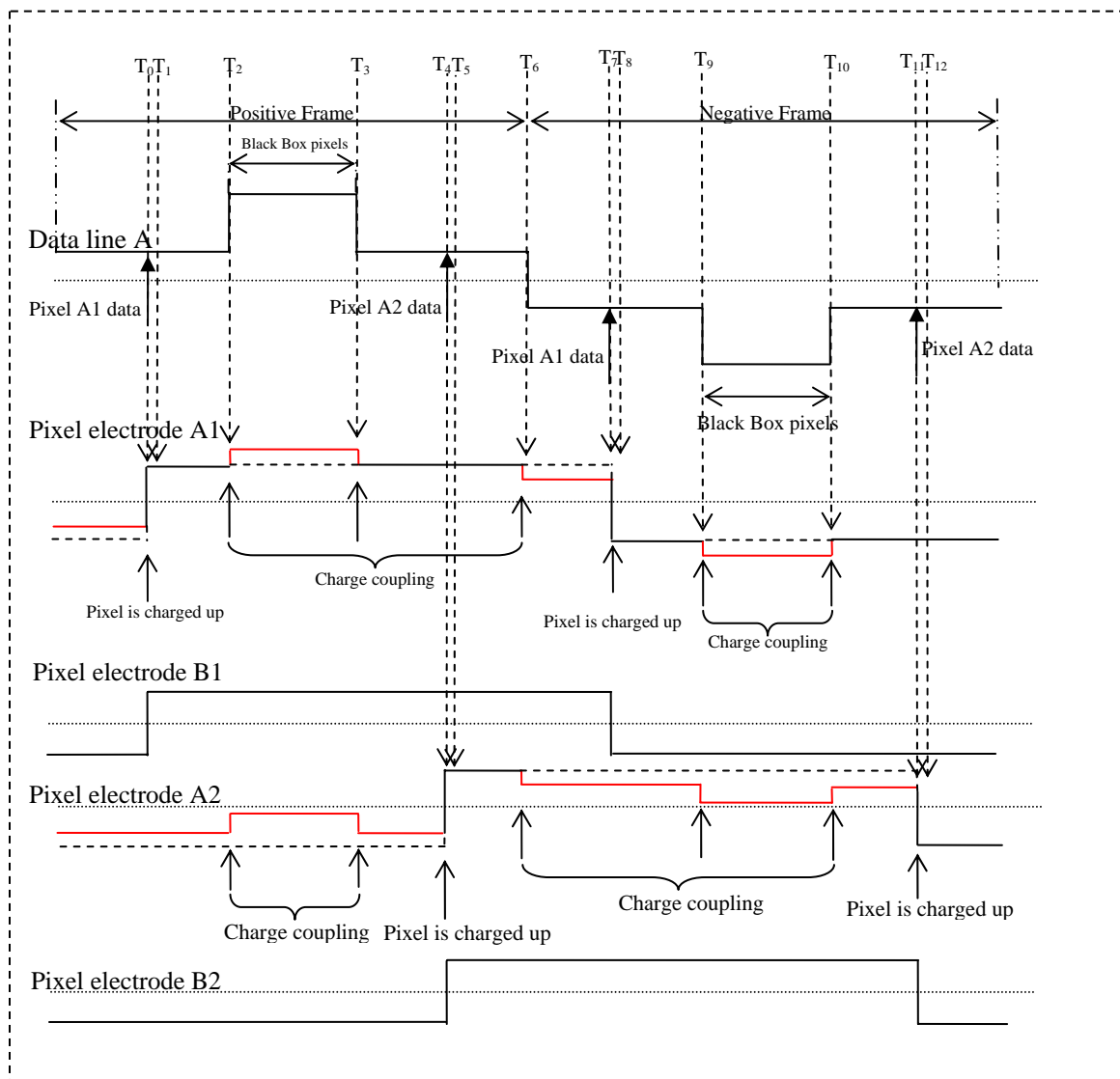
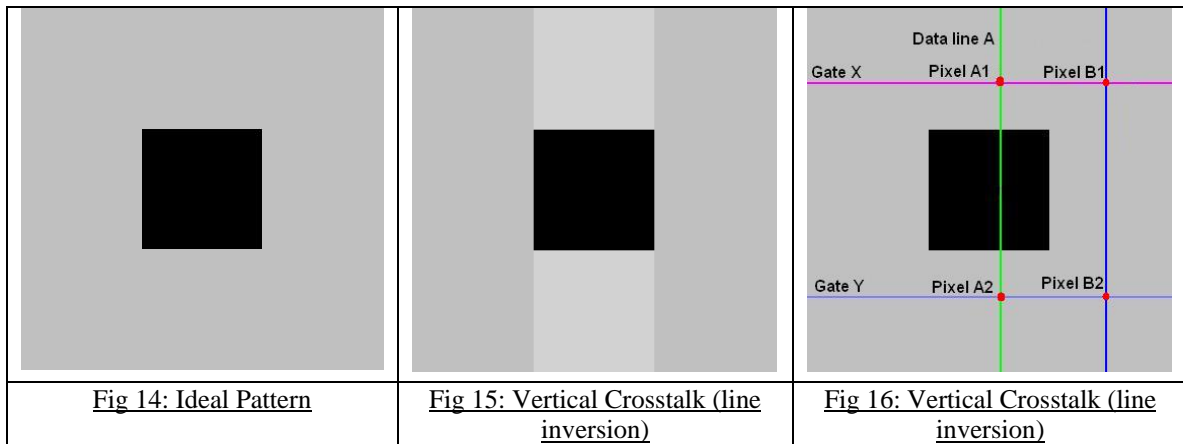


Fig 13: Pixel A1, A2 data which are affected by data line A signal (frame inversion)

### 3.2.1.2. 1-line inversion



- Fig.14 pattern is the ideal pattern without crosstalk effect.
- Fig.15 shows display affected by vertical crosstalk (line inversion)
- Fig.16 shows data line A, B, pixel A1, A2, B1 & B2 location which are used to illustrate vertical crosstalk in line inversion
- Fig.17 shows pixel A1 & pixel A2 electrode voltage which is affected by Data line A
- RMS voltages of pixel electrode A1, A2 are not the same as RMS voltage of pixel electrode B1, B2.
- Contrast is different between A1 & B1, A2 & B2. Actual gray tone depends on display pattern shown.

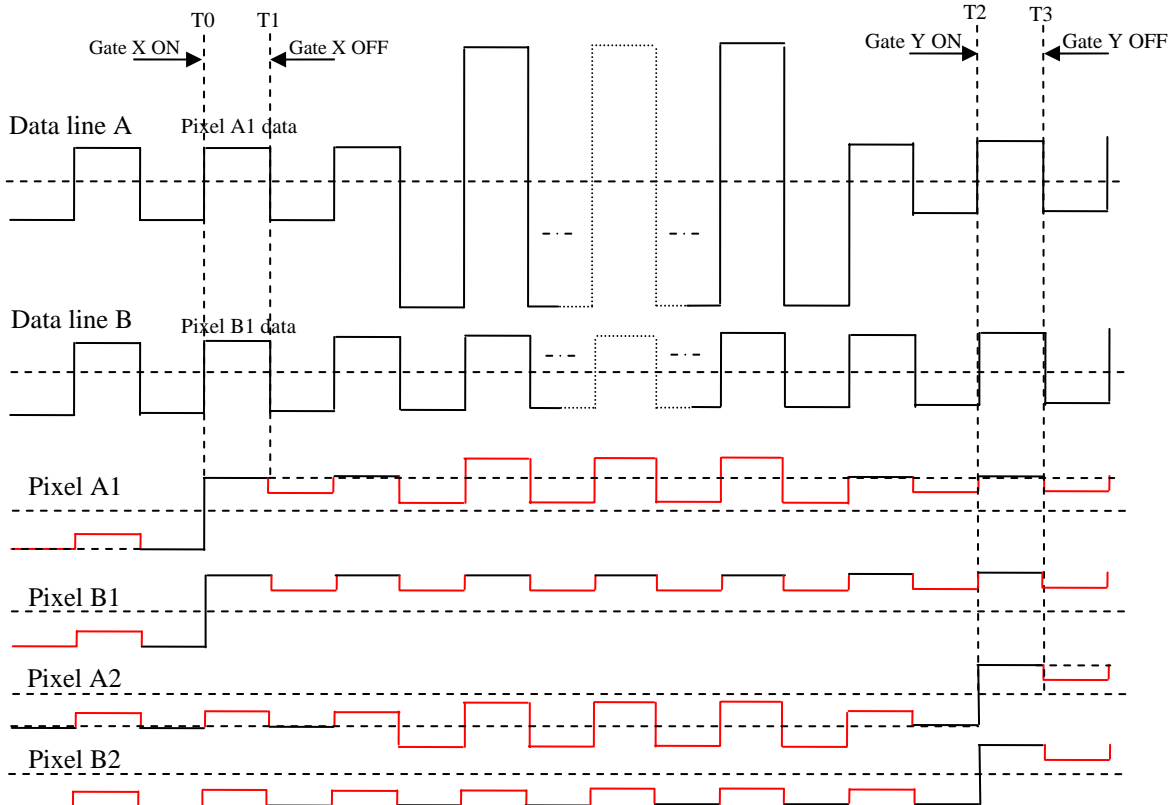


Fig 17: Pixel A1, A2 data which are affected by data line A signal (1-line inversion)

## 4. Solution

### 4.1. Driver IC level

#### 4.1.1. VCIX3 reference for VCOM & VLCD

- In the future, SSL TFT driver products will be added VCIX3 as reference to generate VCOM waveform. This increases VCOM voltage level stability, especially in high loading panel. (panel size

>3.5 inch).

- In these drivers, VCIX3 is also act as a source to generate VLCD. More stable VLCD will increase source voltage reference output stability. This minimizes source voltage output distortion in high loading pattern (e.g. plain gray).

#### 4.1.2. VCOM ON resistance reduction

- VCOM pin ON resistance is carefully taken care in IC design phase of SSL TFT drivers.

#### 4.1.3. Charge sharing on Source

- In most SSL TFT driver products (e.g. SSD2220, SSD2215, SSD1269), Charge sharing in data line (Source) is used. Before every line/frame start, data line will be pre-charged to an intermediate (CDUM0) level Fig. 18. Longer rise/fall time of source minimizes effect of capacitive coupling to VCOM waveform, in additional to power saving.

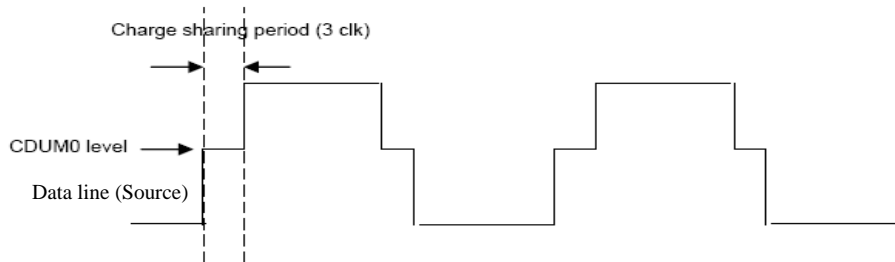


Fig 18. Charge sharing in data line in SSL product

Fig 19. Charge sharing in VCOM in SSL product

#### 4.1.4. Dot inversion & column inversion

- In the future, SSL TFT drivers, which will support high resolution, will feature with DC VCOM with column & dot inversion. When every gate turns ON, there are always equal numbers of data lines (source) have positive & negative polarity. Capacitive coupling effect will be cancelled out each other. We use 1-line column inversion as an example. Data line A1 & A2 (location shown in fig 20) are data line which is adjacent to each other. In 1-line column inversion, adjacent data line (e.g. A1 & A2) have signal which is always out of phase with each other (provided that display content of these 2 lines is the same) as shown in fig 21. Capacitive coupling caused by these data line will then be cancelled out with each other. Similar phenomenon happens in dot inversion driving mode.

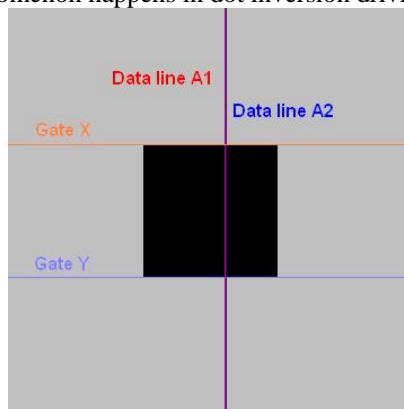


Fig 20. Location of Data line A1 & A2 in illustration of column inversion

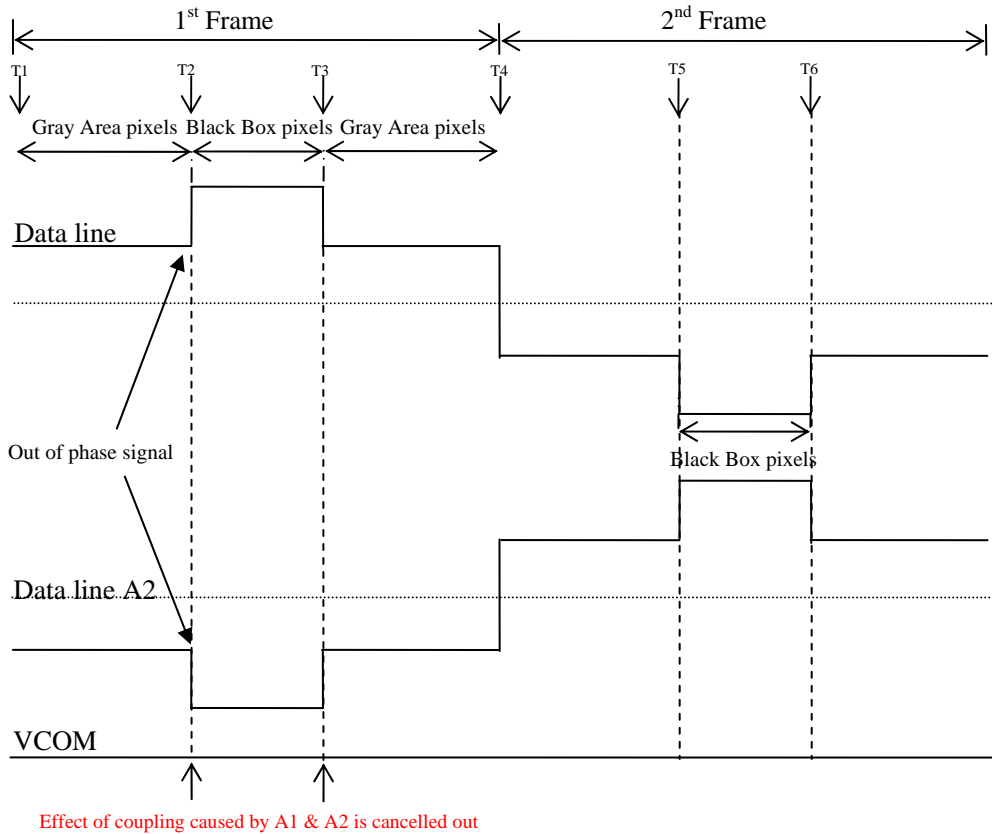


Fig 21. Data line & VCOM waveform in column inversion

#### 4.2. Panel level

- Minimize parasitic capacitance between VCOM & Source in panel layout.
- Minimize parasitic capacitance between Source & pixel electrode in panel layout.
- Minimize ITO resistance on VCOM & Source pin. Suggested Source pin & VCOM pin resistance are < 100 ohms & <10 ohms respectively. Fig.22 & Table 1 below shows an example of ITO resistance requirement on input pins.

Figure 19-4 - ITO and FPC connection example

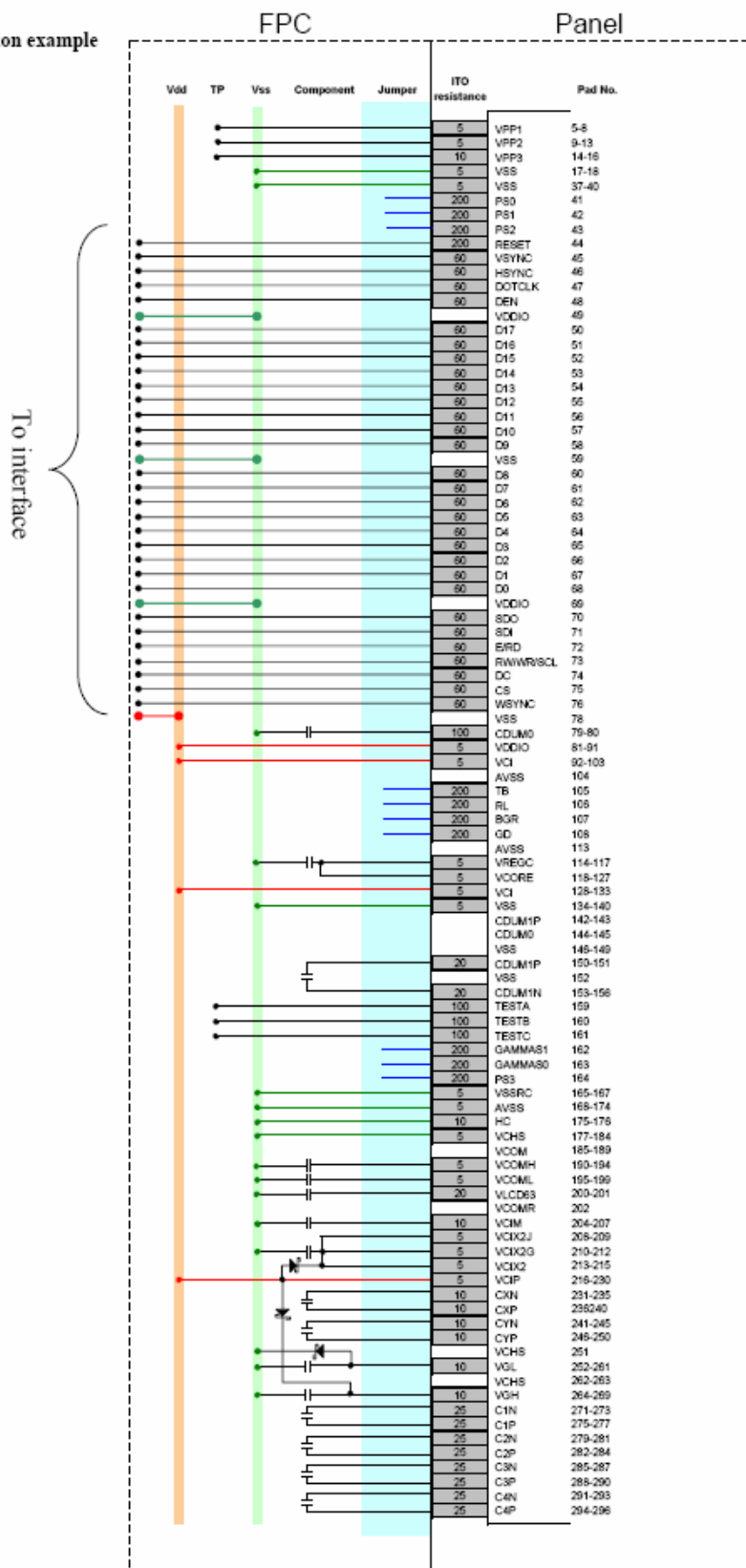


Fig 22. Suggested ITO resistance requirement on panel layout

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